

Appl. No. 09/451,196
Amdt. Dated May 13, 2005
Reply to Office action of January 13, 2005

REMARKS/ARGUMENTS

Claims 1-31 are pending in the present application.

This Amendment is in response to the Office Action mailed January 13, 2005. In the Office Action, the Examiner rejected claims 1-31 under 35 U.S.C. §102(e). Applicants have amended claim 17. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Claim Objection

1. In the Office Action, the Examiner objected to claim 17 due to informalities. In response, Applicants have amended claim 17 to add the missing word "table". Accordingly, Applicants request the objection be withdrawn.

Rejection Under 35 U.S.C. § 102

2. In the Office Action, the Examiner rejected claims 1-31 under 35 U.S.C. §102(c) as being anticipated by U.S. Patent No. 6,359,897 issued to Bergantino et al. ("Bergantino"). Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of anticipation.

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergasaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Bergantino discloses an asynchronous transfer mode cell processing system with scoreboard scheduling. A primary scoreboard 100 represents the cell schedule and includes a group of bits arranged in a number of 16-bit lines (Bergantino, col. 16, lines 57-59). A connection ID table 110 includes a 16-bit entry for each of the bits in the primary scoreboard (Bergantino, col. 16, lines 62-64). Each entry in the connection ID table 110 represents a cell time slot in a given ATM transmission link, and either contains a connection ID for a given

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schedule VC, or contains no connection ID if the corresponding cell time slot is unscheduled and thus available (Bergantino, col. 17, lines 1-5).

Bergantino does not disclose, either expressly or inherently, (1) a hardware schedule table to schedule connections of traffic in a network having entries corresponding to the connections, (2) N logical schedule tables created from the hardware schedule table, (3) the N logical schedule tables being separated by table delimiters and operating independently of one another, (4) each of the table delimiters corresponding to at least one unused entry in the hardware schedule table, and (5) an identifier being assigned to an available entry in one of the N logical schedule tables.

Bergantino merely discloses a connection ID table to represent cell time slots and a scoreboard to contain bits corresponding to the entries in the connection ID table. Neither the connection ID table nor the scoreboard is the same as the N logical schedule tables in many aspects. First, the connection ID table contains entries representing cell time slots and the scoreboard contains bits corresponding to the entries. They not created from a hardware schedule table. Second, there is only one connection ID table and one scoreboard, not N logical schedule tables. Third, the Bergantino connection ID table and the scoreboard work together, because the number of bits in the primary scoreboard 100 equals the number of entries in the connection ID table 110 (Bergantino, col. 17, lines 30-32). Therefore, they are not operating independently of one another. Fourth, there are no table delimiters separating the N logical schedule tables. The connection ID table contains entries and the scoreboard contains bits corresponding to the entries. The entries are either available or the scheduled VC (Bergantino, col. 17, lines 30-32; Figure 4, elements 100 and 110). These entries and bits are not table delimiters that separate the N logical tables. Fifth, even if table delimiters were disclosed, there was no correspondence between the delimiters and at least one unused entry in the N logical schedule tables.

The Examiner states that Bergantino discloses the N logical schedule tables being separated by table delimiters and operating independently, citing Bergantino, column 17, lines 23-35. However, no such table delimiters are disclosed in the cited paragraph which is reproduced below for ease of reference:

“The boundary of the periodic container relative to the transmission convergence framing structure is generally arbitrary. Each location or cell time slot within the periodic container in the

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exemplary embodiment of FIG. 4 corresponds to a single bit in the primary scoreboard 100 and thus a single entry in the connection ID table 110. The number of bits in the primary scoreboard 100 equals the number of entries in the connection ID table 110 and also equals the number of cell time slots in the periodic container. Successive bits in the primary scoreboard 100 and successive locations in the connection ID table 110 represent successive cell time slots on the ATM transmission link.” (Bergantino, col. 17, lines 23-35.)

The cited paragraph merely discloses (1) the correspondence between the bits in the primary scoreboard 100 and the entries in the connection ID table 110, and (2) the correspondence between successive bits and entries in the scoreboard 100 and the connection ID table 110 and the successive cell time slots in the ATM transmission link. Nowhere that logical schedule tables and the delimiters are mentioned in the cited paragraph.

The Examiner further states that Bergantino discloses a scoreboard as the hardware schedule table (Office Action, page 5, paragraph 5). Applicants respectfully disagree. The Bergantino scoreboard only indicates cell schedule operations. A cell time slot is marked as having been scheduled or unscheduled and therefore available for a specific connection if the corresponding primary scoreboard bit is set to a logic 1 or 0, respectively (Bergantino, col. 17, lines 42-45). The Bergantino scoreboard therefore only contains bits 1 or 0 corresponding to whether a cell is scheduled or available. In contrast, the hardware schedule table in the present invention includes the actual entries for the assigned connection identifiers (See, for example, specification, page 8, lines 18-20).

Therefore, Applicants believe that independent claims 1, 9, 17, 25 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejection under 35 U.S.C. §102(e) be withdrawn.

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Conclusion


Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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By



Thinh V. Nguyen

Reg. No. 42,034

Tel.: (714) 557-3800 (Pacific Coast)

12400 Wilshire Boulevard, Seventh Floor
Los Angeles, California 90025

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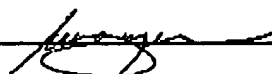
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